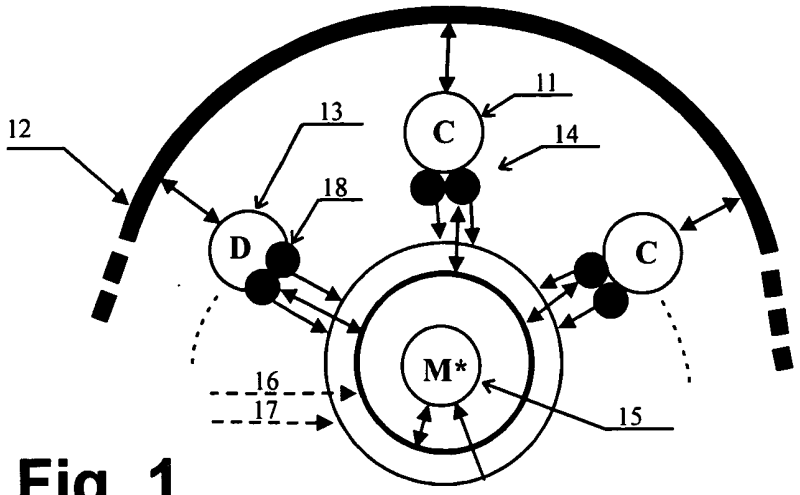

Fig. 1

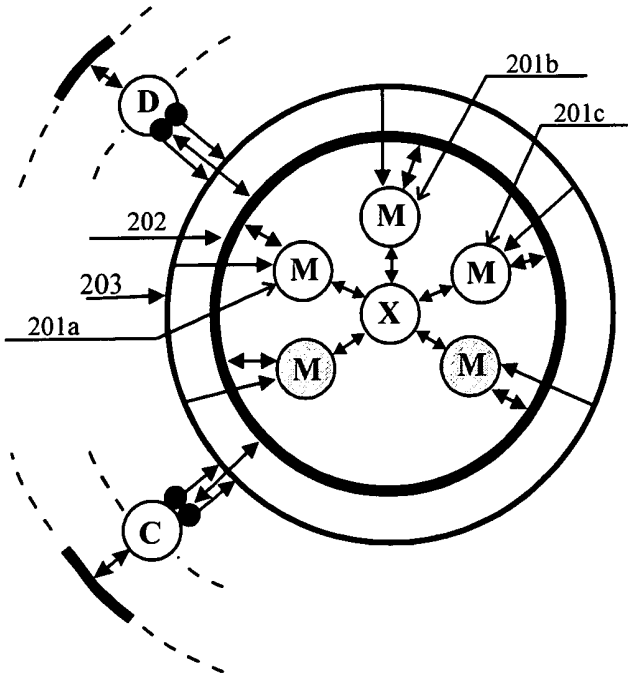

Fig. 2

EXPRESS MAIL LABEL ET 240 951 415 US

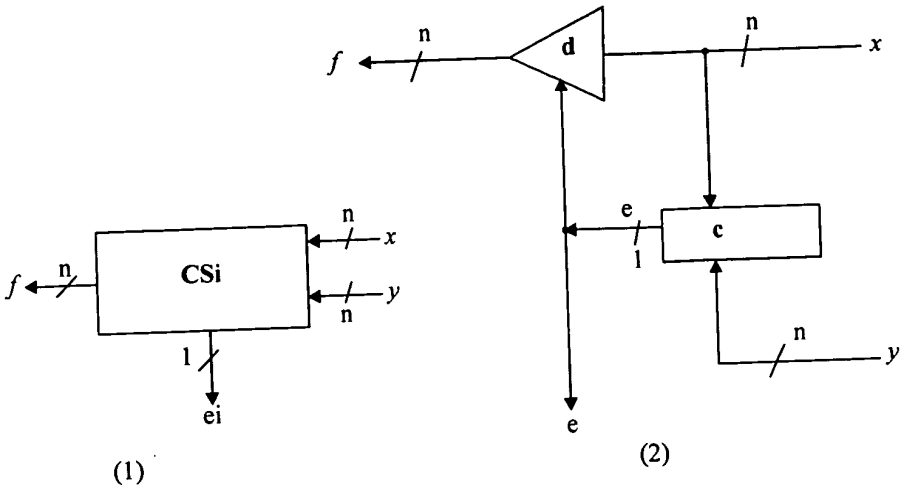
f
n
d
n
x
e
c
l
n
y
e
CSi
f
n
n
x
n
y
l
ei
(1)
(2)

Fig. 3

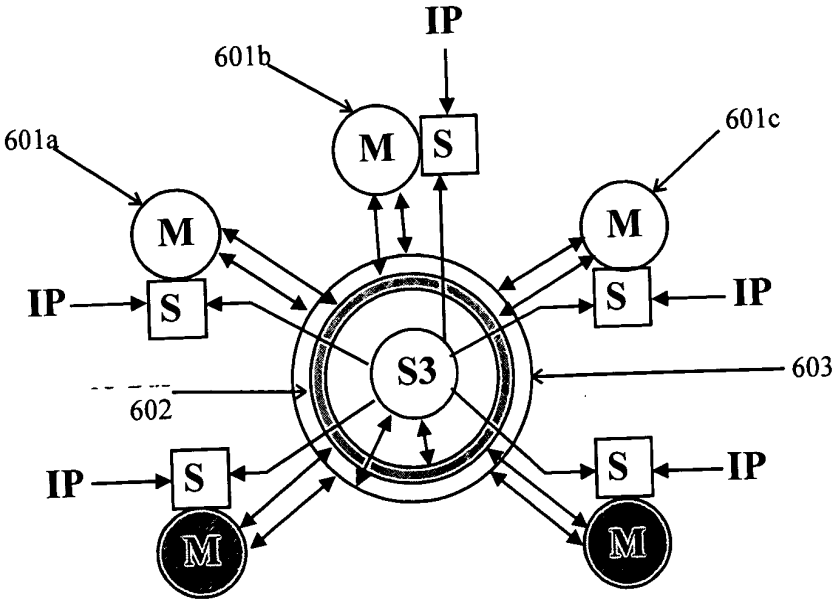
IP
601b
601a
601c
M
S
M
M
IP
S
S
IP
S3
603
602
IP
S
S
IP
M
M

Fig. 6

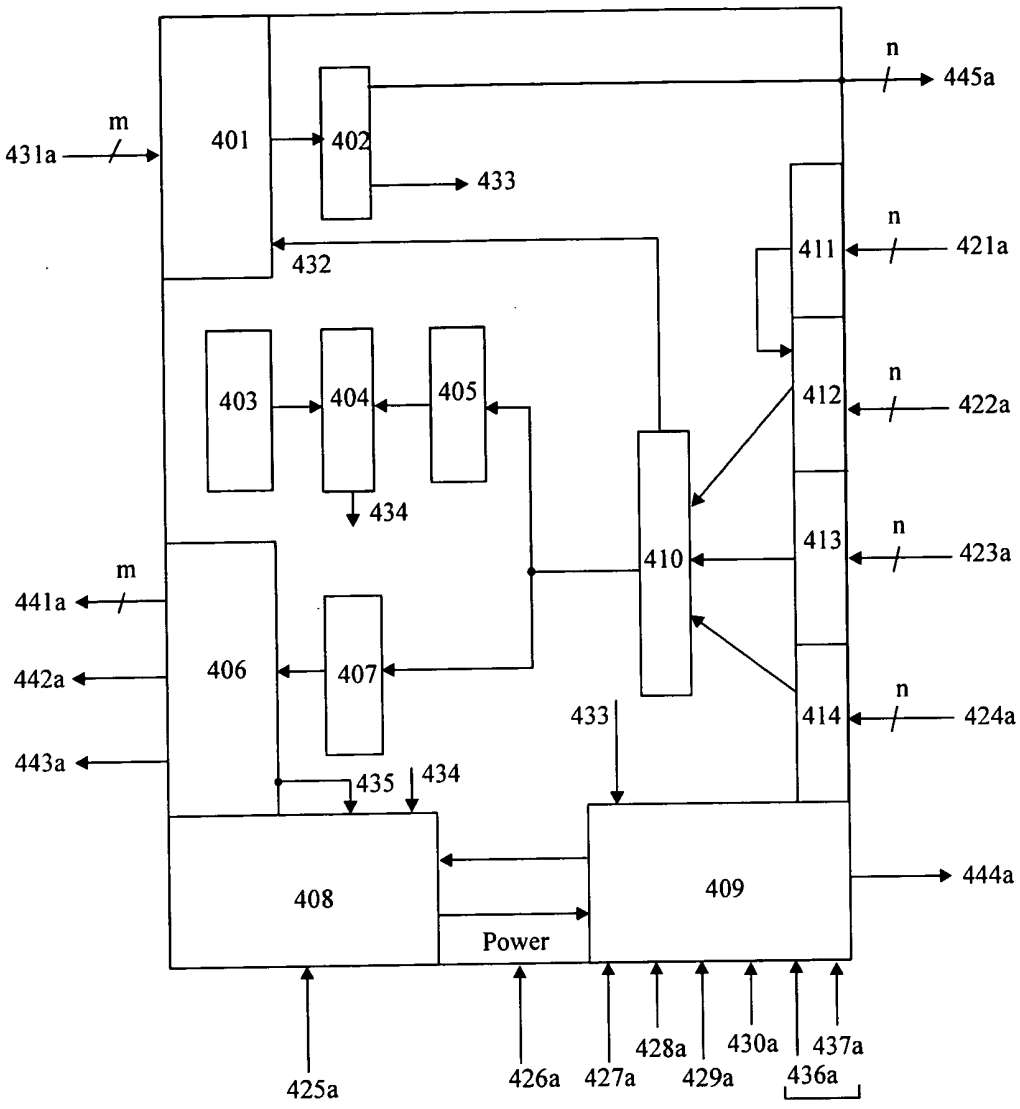
n
445a
m
431a
401
402
433
n
421a
411
432
403
404
405
412
n
422a
434
410
413
n
423a
m
441a
406
407
442a
414
n
424a
433
443a
435
434
408
409
444a
Power
425a
426a
427a
428a
429a
430a
436a
437a

Figure 4a

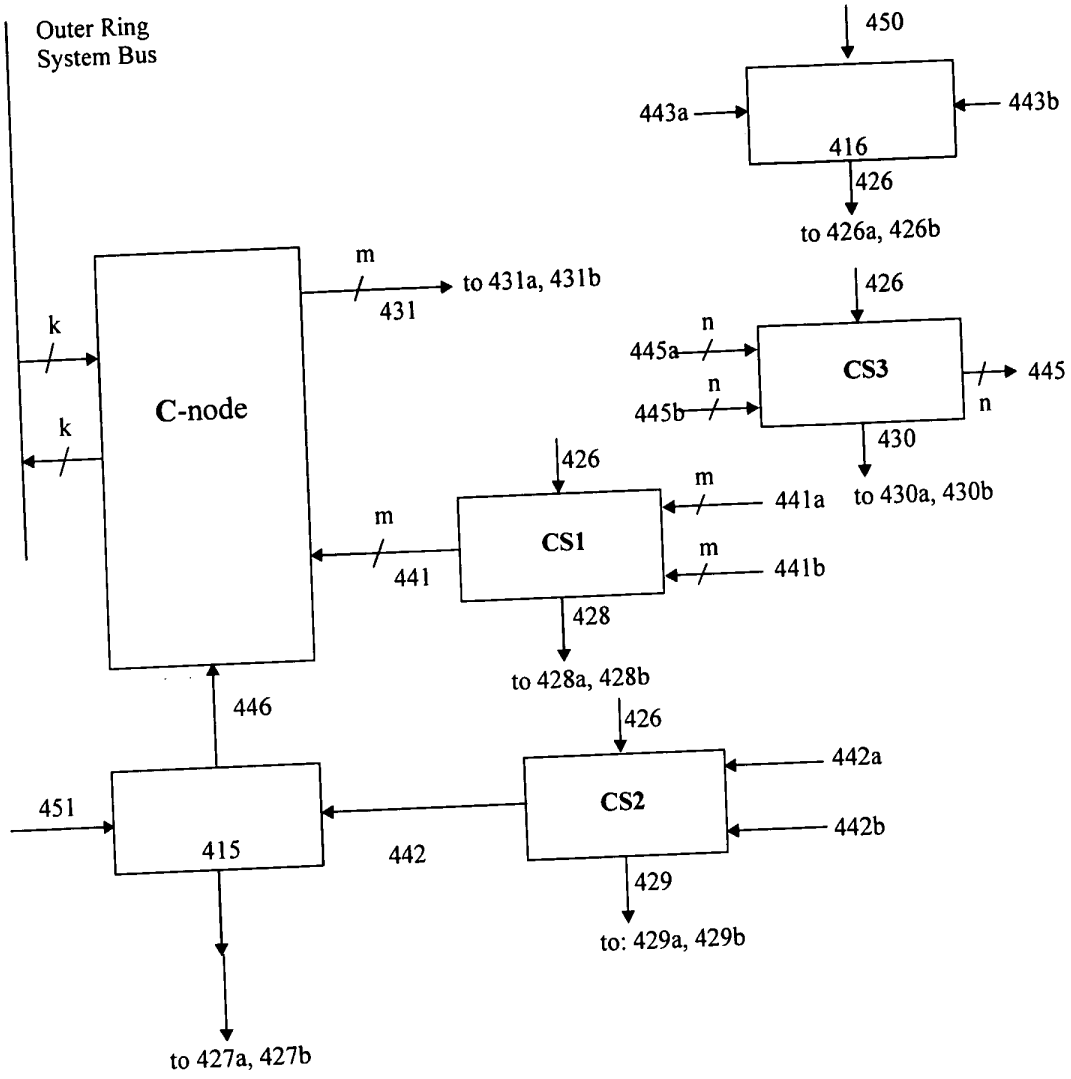
Outer Ring
System Bus
450
443a
443b
416
426
to 426a, 426b
m
to 431a, 431b
431
k
k
C-node
426
n
445a
n
445b
CS3
445
n
430
to 430a, 430b
426
m
441a
m
441b
m
441
CS1
428
to 428a, 428b
446
426
442a
442b
451
415
442
CS2
429
to: 429a, 429b
to 427a, 427b

Fig. 4b

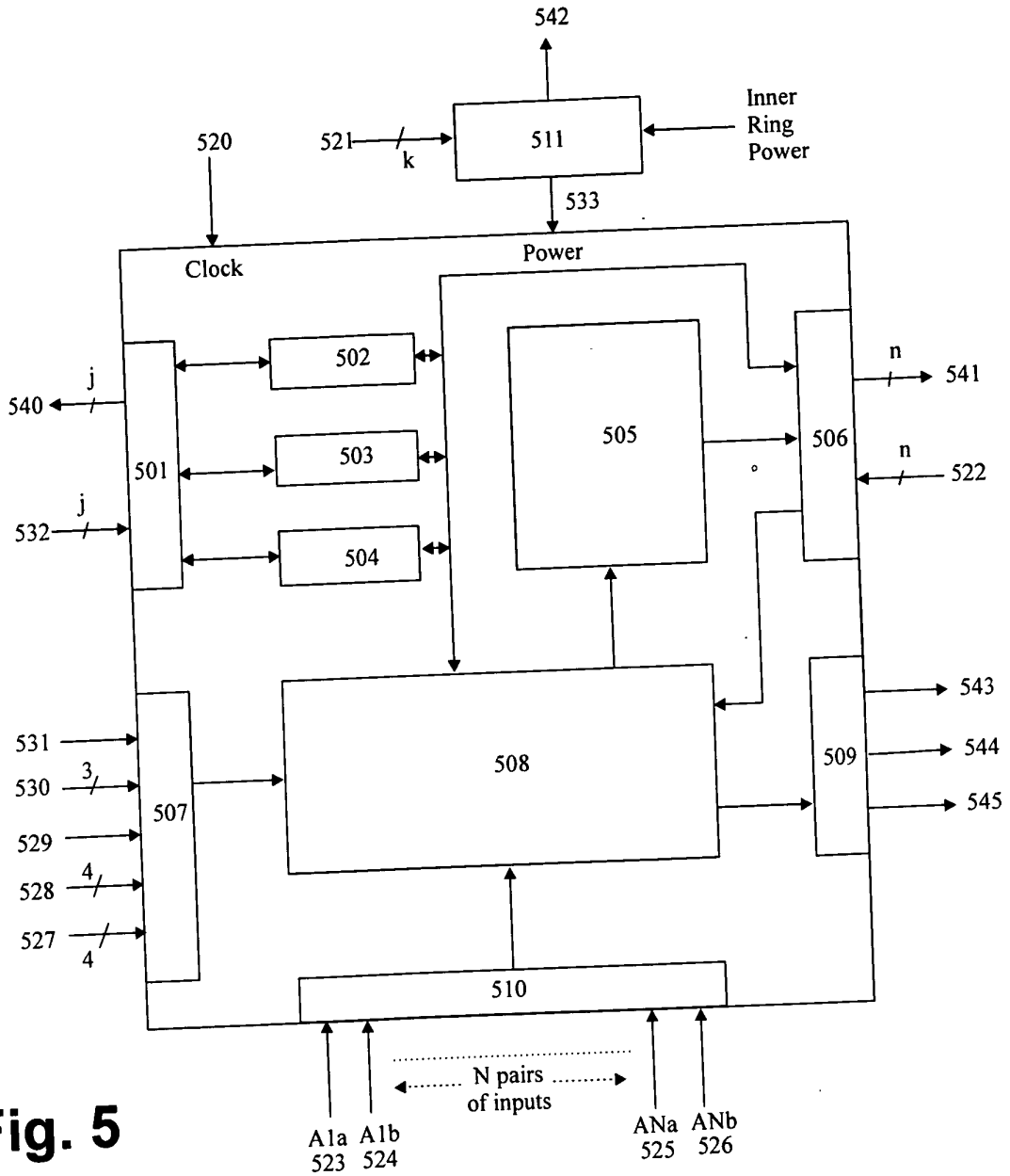
542
Inner
Ring
Power
520
521
k
511
533
Clock
Power
502
503
504
501
505
506
n
541
n
522
j
540
j
532
531
530
3
529
528
4
527
4
507
508
509
543
544
545
510
N pairs
of inputs
A1a
523
A1b
524
ANa
525
ANb
526

Fig. 5

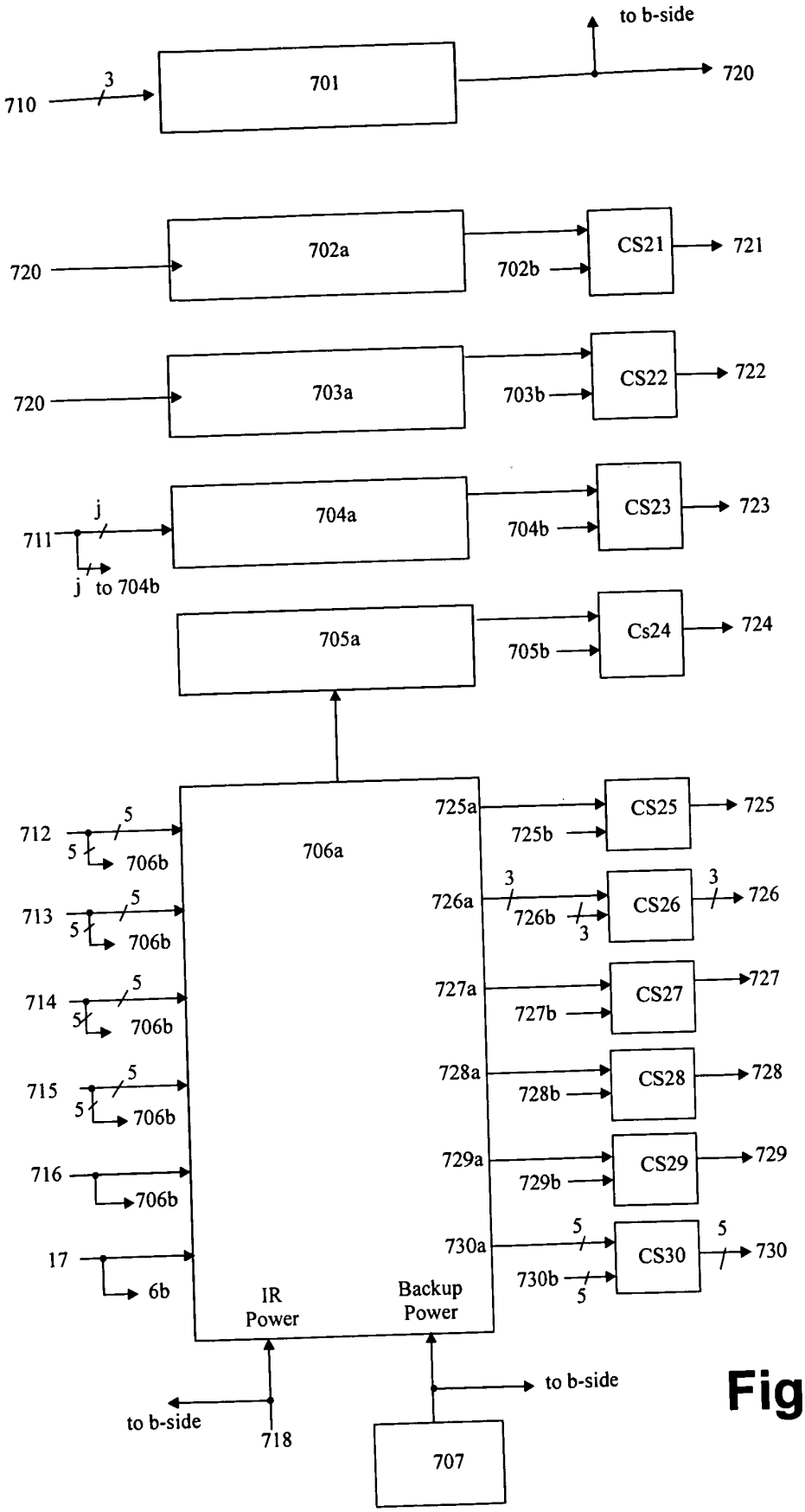
to b-side
710
3
701
720
720
702a
702b
CS21
721
720
703a
703b
CS22
722
711
j
704a
704b
CS23
723
j to 704b
705a
705b
Cs24
724
712
5
5
706b
713
5
5
706b
714
5
5
706b
715
5
5
706b
716
706b
17
6b
706a
725a
725b
CS25
725
726a
3
726b
3
CS26
3
726
727a
727b
CS27
727
728a
728b
CS28
728
729a
729b
CS29
729
730a
5
730b
5
CS30
5
730
IR Power
Backup Power
to b-side
718
to b-side
707

Fig. 7

Figure 8a: Power-On Sequence for the M-Cluster, Controlled by S3-Nodes

(1) S3 nodes switch Power On (Signal 730) for M-node #1, command BIST (Built In Self Test) by signal 725.

(2a) If BIST is OK, keep Power On for #1.

(2b) If BIST fails, Power Off for #1.

(2) The S3 nodes record status ("Good" or "Failed") for #1 in the M-Cluster Status Register MC-SR (705a, 705b).

(3) Repeat steps (1)-(3) until 3 good M-nodes are found, or all M-nodes have been tested, and only 1 or 2 good M-nodes exist.

(4) After 3 good M-nodes are found, Power Off each remaining "Good" node after BIST, record Status as "Spare" in MC-SR.

(6) After all M-nodes have been tested, transfer MC-SR contents (724) via the IC-Bus (602) to the powered good M-nodes.

(7) *Command* TMR, Duplex, or Simplex operation (726) to the M-Cluster. If no good M-nodes were found, send "M-Cluster dead" message (728) to operator.

(8) Switch Power On (729) for all A-nodes (at once). The Inner Ring is now powered and the remaining Power-On steps are controlled by the M-nodes in TMR, Duplex, or Simplex configuration.

(9) Send "Power On in Outer Ring" Command (727) to the M-Cluster.

Figure 8 b: Power-On Sequence for the Outer Ring (one node), Controlled by M-Cluster

This sequence is initiated by the "Power On in Outer Ring" command 727.

(1) Send the "Reset A-pair" command via the M-Bus to A-pair #1.

(2a) If Reset succeeds, "All is well" is received from A-pair #1 and Power On command is sent to the Power Switch of C-node (or D-node) #1. The Power-On command includes C-node (or D-node) BIST command as well.

(2b) If Reset fails, record "Failed" status for C-node #1 in their Outer Ring Status Registers OR-SR (504) of M-nodes, go to (1) for A-pair #2.

(3a) If Power On and BIST both succeed, the M-nodes record "C-node #1 is good" in their OR-SR (504), go to (1) for A-pair #2.

(3b) If either the Power Switch fails to switch on, or BIST fails after power is switched on, record "Failed" in OR-SR for C-node #1., command Power Off if BIST failed, go to (1) for A-pair #2.

Figure 8c: Power-Off Sequence for DiSTARS

(1) S3 nodes switch Power Off (729) for all A-nodes (at once), start Interval Timer (703a).

(2) Removal of A-node power puts the power switches of all C-nodes and D-nodes in the Off position.

(3) S3 nodes switch Power Off (730) for the M-nodes.

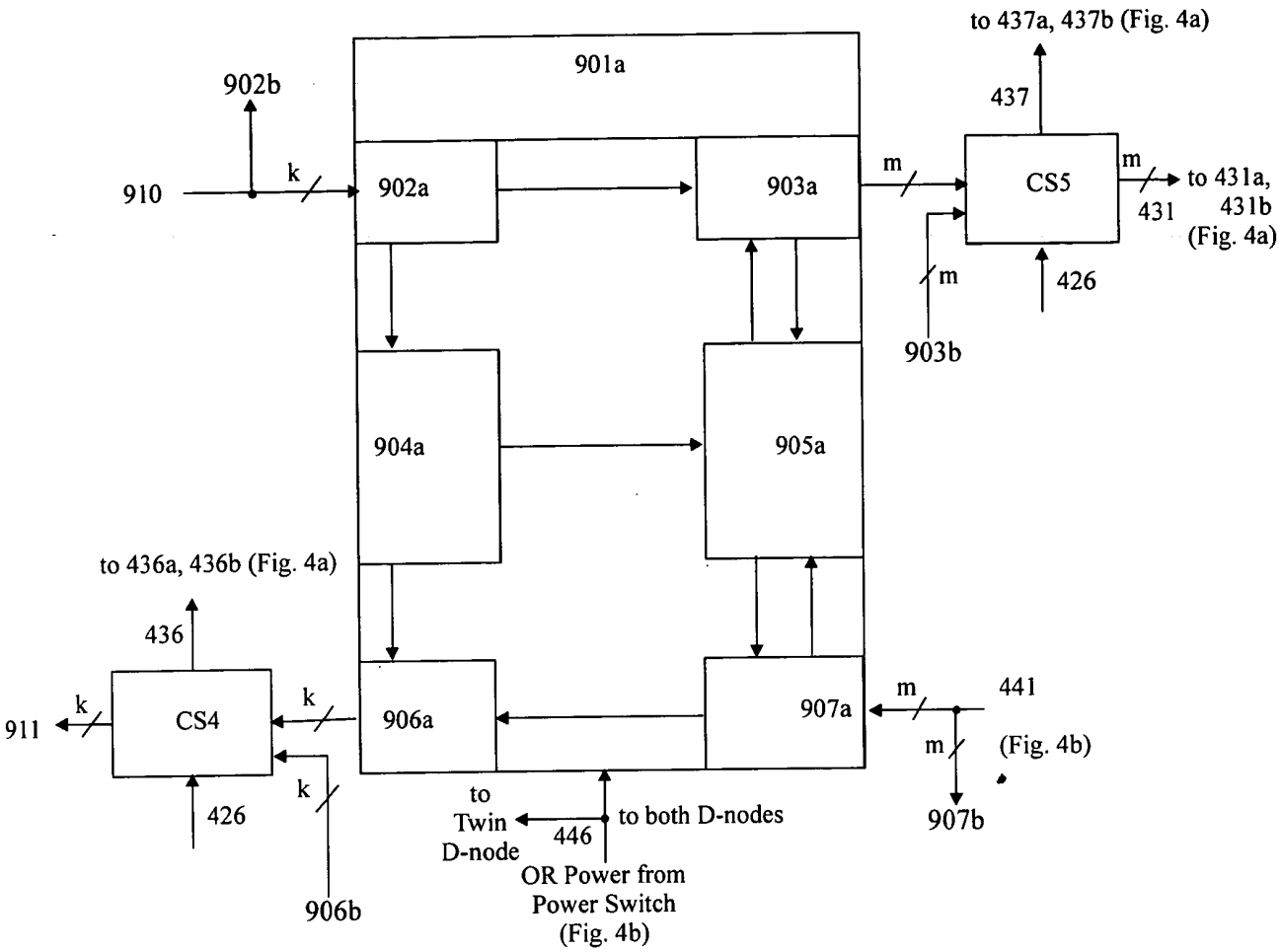
to 437a, 437b (Fig. 4a)
901a
902b
437
910
k
902a
903a
m
CS5
m
to 431a, 431b (Fig. 4a)
431
m
426
903b
904a
905a
to 436a, 436b (Fig. 4a)
436
911
k
CS4
k
906a
907a
m
441
m
(Fig. 4b)
907b
426
k
906b
to Twin D-node
446
to both D-nodes
OR Power from Power Switch (Fig. 4b)

Fig. 9

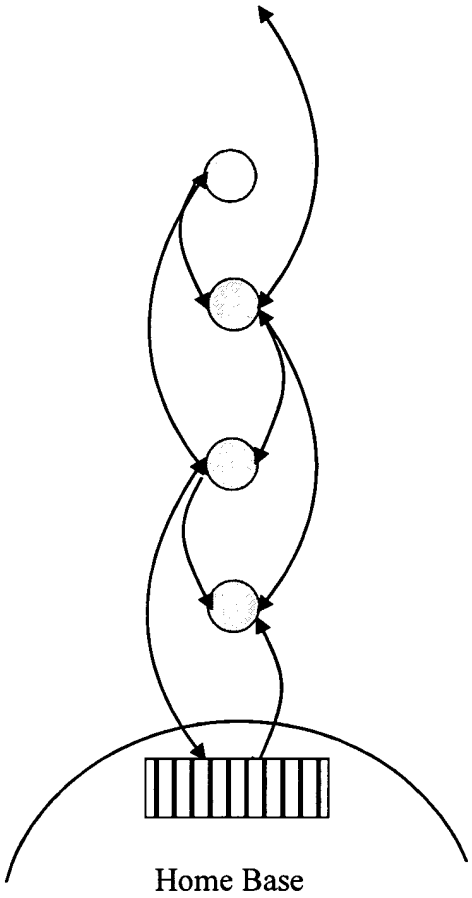

Fig. 10